Amendments to the Specification

Please substitute the paragraph starting on page 13, line 29 and continuing to page 14, line 5 of the present specification with the following paragraph:

Referring to FIG. 8, multiplication operations are implemented using a finite state machine. Multiplication begins in IDLE state 8010. The multiplier stays in the idle state until the start signal is asserted. Then, the multiplier transitions to either the ARR1 state 8020 or the ARR2A state 8030 depending on whether operand RT contains a 32-bit or 16-bit value. If a ~~16-bit~~ 32-bit value is stored in RT, then the system transitions to state ARR2B 8040 where the second array pass is run. If a 16-bit value is stored in operand RT, the multiplication is run through the array unit in state ARR1 8020.